

Amendments to the Claims:

The below listing of claims will replace all prior versions in this application. Please amend the claims as indicated below.

1. (Currently Amended.) A method for fabricating a semiconductor device, comprising the steps of:

sequentially forming a buffer layer and an interlayer insulating film on a semiconductor substrate;

etching the interlayer insulating film and the buffer layer to form a contact hole exposing the semiconductor substrate;

performing a cleaning process of a lower portion of the contact hole;

~~doping an impurity into the surface of the semiconductor substrate exposed by the contact hole;~~

ion-implanting an impurity into the lower portion of the contact hole;

doping an impurity gas into a surface of the semiconductor substrate exposed by the contact hole, wherein PH_3/N_2 gas is used for the impurity gas; and

forming a conductive layer filling the contact hole on the entire surface of the resulting structure.

2. (Original.) The method of claim 1, wherein the buffer layer comprises a nitride film.

3. (Original.) The method of claim 1, wherein the interlayer insulating film comprises an oxide film.

4. (Original.) The method of claim 1, wherein the cleaning process comprises sequentially performing a dry cleaning process for removing a portion damaged during the contact hole etching process, and a wet cleaning process for removing carbon composite residues and a native oxide film.

5. (Currently Amended.) The method of claim 4, wherein the dry cleaning process is performed using a plasma of mixture gas of NH_3 , O_2 , $[[\text{HE}]]$ He and N_2 for 1 to 5 minutes with a bias power ranging from 1 to 10kW in the direction of the semiconductor substrate.

6. (Original.) The method of claim 4, wherein the dry cleaning process is performed using a plasma of mixture gas of NH_3 and N_2 , and the resulting structure is further subjected to an annealing process for 1 to 10 minutes at a temperature ranging from 100 to 500°C.

7. (Original.) The method of claim 4, wherein the wet cleaning process is performed using a solution selected from the group consisting of H_2O_2 , H_2SO_4 , NH_4OH , HF , BOE solutions, and combinations thereof as a cleaning solution.

8. (Cancelled.) The method of claim 1, wherein the step of doping an impurity into the surface of the semiconductor substrate is performed by ion-implanting an impurity into the lower portion of the contact hole;

9. (Currently Amended.) The method of claim $[[8]]$ 1, wherein the ion-implanting process is performed by implanting P or As having a dose ranging from $1\text{E}10$ to $1\text{E}20$ atoms/ cm^2 with an implantation energy ranging from 10 to 100keV.

10. (Cancelled.) The method of claim 8, wherein the ion-implanting process further comprises exposing the surface of the semiconductor substrate exposed by the contact hole to a PH_3/N_2 gas atmosphere to diffuse P into the exposed the semiconductor substrate.

11. (Currently Amended.) The method of claim $[[10]]$ 1, wherein the surface of the semiconductor substrate is exposed to PH_3/N_2 gas atmosphere for 5 to 60 minutes under a pressure ranging from 0.1 to 10 Torr and at a temperature ranging from 400 to 700°C.

12. (Original.) The method of claim 1, wherein the conductive layer consists of a polysilicon layer formed in a low pressure chemical vapor deposition process using a mixture gas of mono silane (MS), PH_3 and N_2 as a reaction gas under a pressure ranging from 0.1 to 10 Torr and at a temperature ranging from 400 to 700°C.

13. (Original.) The method of claim 12, wherein the flow rate of mono silane ranges from 500 to 5000 sccm.
14. (Original.) The method of claim 12, wherein the flow rate of N₂ ranges from 100 to 5000 sccm.
15. (Original.) The method of claim 12, wherein the H₂ gas contains 1% of PH₃ gas and has a flow rate ranging from 10 to 1000 sccm.
16. (Original.) The method of claim 1, wherein a thickness of the conductive layer ranges from 1000 to 5000Å.
17. (Original.) The method of claim 1, wherein the conductive layer consists of a polysilicon layer having 1.0E19 to 3.0E20 atoms/cc of P therein.
18. (Currently Amended.) The method of claim 1, wherein the impurity concentration of the conductive layer from the contact interface to a height ranging from 50 to 500Å ranges from 1.5E20 to 3.0E20 atoms/cc.